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(54) Title: ELECTRONIC DEVICES WITH BARRIER FILM AND PROCESS FOR MAKING SAME

(54) Titre: DISPOSITIFS ELECTRONIQUES POURVUS DE FILMS BARRIERES ET PROCEDE DE FABRICATION

## (57) Abstract

A semiconductor device having a barrier film (47) comprising an extremely thin film formed of one or more monolayers each comprised of a two-dimensional array of metal atoms. In one exemplary aspect, the barrier film (47, 49) is used for preventing the diffusion of atoms of another material (45) such as copper conductor, into a substrate (46), such as a semiconducting material or an insulating material, and an oxide layer (48). Methods for making the barrier film (47) in a semiconductor device are also covered. The extremely thin barrier film (47, 49) makes possible a significant increase in the component density and a corresponding reduction in the number of layers in large scale integrated circuits, as well as improved performance.

## (57) Abrégé

Ce dispositif à semi-conducteurs est pourvu d'un film barrière (47) constitué d'une pellicule extrêmement mince formée d'une monocouche, sinon de plusieurs, faites, chacune, d'un réseau bi-dimensionnel d'atomes de métal. Dans un mode de réalisation, donné à titre d'exemple, on utilise le film barrière (47, 49) pour empêcher la diffusion d'atomes d'une autre matière (45), un conducteur en cuivre notamment, dans un substrat (46) tels qu'un matériau semi-conducteur ou isolant, et dans une couche d'oxyde (48). L'invention a également trait à des procédés de fabrication de ce film barrière (47) dans un dispositif à semi-conducteurs. La présence de ce film barrière extrêmement mince (24, 54) permet d'accroître la densité du composant et de réduire, de façon corollaire, le nombre de couches dans des circuits intégrés de grande taille ainsi que d'améliorer les caractéristiques de fonctionnement.

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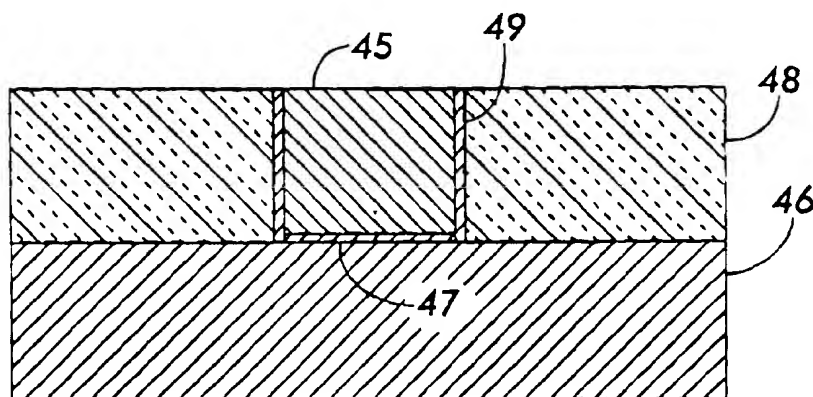
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(54) Title: ELECTRONIC DEVICES WITH BARRIER FILM AND PROCESS FOR MAKING SAME



(57) Abstract

The present invention relates to a barrier film for use in electronic devices. The barrier film is formed by a process that includes depositing a layer of a material having a high degree of purity and a high degree of uniformity. The barrier film is then subjected to a process that increases its density and its corresponding adhesion to the substrate. The barrier film is then used in the manufacture of large scale integrated circuits as well as improved performance.

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## Description

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DescriptionELECTRONIC DEVICES WITH BARRIER FILM  
AND PROCESS FOR MAKING SAMEStatement of Government Interest

The invention described herein may be manufactured and used by or for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

Technical Field

This invention relates generally to the fabrication of electronic devices, and particularly to a novel barrier film for electronic and electro-optic materials.

Background Art

Integrated circuits (ICs) are composed of many millions (sometimes billions) of components such as transistors, resistors, and capacitors. These individual components are laid out in a two dimensional array on a substrate such as silicon or gallium arsenide. The two dimensional arrays are often stacked one on top of another to form a three dimensional IC. As in any circuit, these components, and the several layers, must be connected to one another electrically. Interconnection on the two dimensional surfaces is accomplished by depositing strips of metal that act as connecting "wires." Likewise, the layers are interconnected by metal plugs deposited in via holes made between layers. These steps in the manufacturing process are commonly referred

5 to as "metallization."

10 Generally, silicon is the substrate material of choice,  
aluminum is the metal of choice for two dimensional IC  
metallization, and tungsten is the metal of choice for filling  
5 via holes for multiple layer interconnection. Silicon is  
15 preferred because it is cheap and abundant. Aluminum and  
tungsten are chosen because they have adequate electrical  
conductivity and they can be made not to diffuse into the  
20 substrate during the many annealing operations inherent in the  
10 IC manufacturing process.

25 Because the electrical conductivity of aluminum and  
tungsten is limited, the "wires" and plugs must be made thick  
enough to ensure minimal resistance to electric current  
between components and between layers. The large size of  
30 15 these conductors has recently become an issue for IC designers  
and fabricators interested in placing a greater density of  
circuit elements on an IC. In order to achieve greater  
35 performance from ICs, the lateral dimensions of the circuit  
elements must be reduced. This reduction in IC element size  
20 has two detrimental effects on the resulting IC. First, it  
40 increases the resistance of the metal interconnects. Second,  
it increases the aspect ratio of the via holes, making them  
45 more difficult to fill with the metallic material. Incomplete  
filling of the via holes exacerbates the problem of high  
25 resistance. Today, there is often not enough space in the  
lateral direction on an IC chip to accommodate large aluminum  
50 conductors. Additionally, the size of the via holes, when

5 filled with tungsten, limits the number of levels in the IC to  
no more than five.

10 Copper, which is a much better conductor of electricity  
than aluminum, is available as an alternative metallization  
5 material. Because of copper's greater electrical  
conductivity, copper imposes less resistance to the flow of  
15 electrons than aluminum or tungsten conductors having  
equivalent dimensions. The increasing density of components  
on today's ICs requires the smaller sized conductors that are  
20 only achievable by the use of highly conductive metallization  
10 materials.

25 Unfortunately, copper has one notable problem. It has a  
tendency to diffuse into silicon at elevated temperatures.  
This has precluded copper as a metallization candidate because  
30 15 ICs must be annealed several times during the manufacturing  
process. In order for copper metallization to be feasible, a  
technique must be developed that will prevent the diffusion of  
35 copper into silicon. Among the possible solutions currently  
under development within the semiconductor industry the most  
20 prevalent is the use of nitrides of the transition metals  
40 titanium and tungsten. The thickness of the metal-nitride  
layer required to stop copper diffusion into silicon  
effectively is in the range of tens to hundreds of nanometers,  
45 or hundreds to thousands of Angstroms (Å).

25 The problem of diffusion exists not only in the case of  
copper metallization on silicon, but also in the case of  
50 copper metallization on other single- and polycrystalline

5 semiconductor substrate materials such as gallium arsenide,  
silicon carbide, germanium, and so forth. Copper diffusion  
10 into insulating materials such as  $\text{SiO}_2$  can also result in short  
circuits, especially in dense arrays of IC components.

5 Diffusion is also a problem with other high conductivity  
15 metallization materials such as gold, silver, and platinum.

An object of this invention is to provide a barrier film  
which is extremely thin, yet permits metallization using  
20 copper and other high conductivity metallic conductors which  
10 would otherwise have a tendency to diffuse into a substrate  
formed of a semiconducting or insulating material.

25 It is also an object of the invention to improve  
electronic and electro-optic devices by making it possible to  
achieve one or more of the following desirable  
30 15 characteristics: increased component density in large scale  
integration, reduced heat dissipation, increased speed of  
operation, and a decreased number of layers.

35 Still another object is to provide a procedure for  
forming an extremely thin diffusion barrier, which produces  
20 consistent results rapidly and reliably, and which is not  
40 highly dependent upon the accurate maintenance of operating  
conditions such as time and temperature.

45 Still another object is to provide a process for forming  
an extremely thin diffusion barrier which eliminates voids and  
25 mechanical stresses that can have detrimental effects on the  
substrate, the diffusion barrier, or the metallization layer.  
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**Disclosure of the Invention**

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In accordance with this invention, a semiconductor device is fabricated by forming, on a surface of a substrate material, a barrier film having a monolayer of metal atoms immediately adjacent the surface of the substrate material. In one aspect, a metallic conductor, which has a tendency to diffuse into the substrate material, is then deposited onto the barrier film. Metallic conductors which have a tendency to diffuse into substrates of semiconductor or insulating materials include, for example, pure copper, copper alloys (e.g., Cu-Al, Cu-Si-Al), copper doped with a dopant (e.g., aluminum) that impedes electromigration, gold, silver, or platinum. For purposes of this invention, a "monolayer" is understood to refer to a two-dimensional array of atoms having the thickness of one atomic layer; although the monolayer may have minuscule defects such as minute portions with a thickness that exceeds one atomic layer and/or minute portions that are voids, the average thickness nonetheless essentially is an atomic layer providing essentially complete coverage of the directly underlying substrate surface regions. The monolayer, which is extremely thin by definition, serves as a barrier film, inhibiting diffusion of the metallic conductor into the substrate material. For purposes of this application, the material upon which the monolayer of atoms is formed is often generally referred to herein as a "substrate" for such formation, and it will be appreciated that the term "substrate" as used herein can encompass a bulk wafer or, alternatively, a layer that is

5 grown, deposited, formed or bonded upon another body. The  
present invention is especially concerned with substrates that  
10 are semiconductor or insulating materials.

In one preferred method of this invention, a monolayer is  
5 produced by depositing a metal halide upon a surface of a  
semiconducting or insulating substrate material where it first  
15 reacts with the substrate material and dissociates, releasing  
gaseous by-products formed of substrate atoms and halogen atoms  
20 of the precursor compound. This reaction is self-limiting  
resulting in formation of a monolayer of metal atoms on the  
substrate that thereafter enables a homoepitaxial film formed  
25 of the metal halide molecules to form thereon as the deposition  
process proceeds. This deposition operation can be carried out  
by various methods, but is preferably carried out by molecular  
30 beam epitaxy, or alternatively by r.f. sputtering. At this  
junction, a temporary heteroepitaxial film has been formed on  
the substrate where the diffusion barrier is ultimately  
35 desired. Then, in a second stage of the procedure, the  
temporary heteroepitaxial film is subjected to a selective  
20 removal procedure, whereby the homoepitaxial portion of the  
40 deposited film having the halogen constituents is selectively  
eliminated while the monolayer of metal atoms remains behind  
attached to the surface of the substrate material. The removal  
45 procedure preferably is an annealing operation. Alternatively,  
25 chemical etching which is selective to remove the homoepitaxial  
portion of the deposited film while leaving the monolayer of  
50 metal atoms also can be used. In any event, the metal atom

5 monolayer strongly adheres to the substrate material, and is  
not adversely affected by extended annealing times, high  
annealing temperatures, or chemical etching conditions.

10 The precursor compound preferably comprises a metal  
5 halide, e.g., a barium, strontium, cesium or rubidium- halide  
salt. The thickness of the monolayer basically corresponds to  
15 the diameter of the metal atom constituent(s) of the monolayer.  
Metal atoms of barium, strontium, cesium, rubidium, and so  
20 forth have a thickness (i.e., the diameter of the largest  
10 electron orbital) of less than 5 Å, so it can be appreciated  
that an extremely thin diffusion barrier layer is achieved by  
this invention. The semiconducting substrate materials that can  
25 be processed according to this invention include mono- or  
polycrystalline, doped or undoped, semiconductors, such as  
30 15 silicon, germanium, indium phosphide, gallium arsenide, silicon  
carbide, gallium nitride, aluminum nitride, indium antimonide,  
lead telluride, cadmium telluride, mercury-cadmium telluride,  
35 lead selenide, lead sulfide, tertiary combinations of these  
materials, and so forth. The insulating substrate materials  
20 that can be processed according to this invention include doped  
40 or undoped silicon oxides (e.g., silicon dioxide), silicon  
nitride, phosphosilicate glass (PSG), borophosphosilicate glass  
(BPSG), barium fluoride, strontium fluoride, calcium fluoride,  
45 and so forth.

25 In a further embodiment of this invention, a multiplicity  
of monolayers are formed contiguous with each other upon the  
50 substrate surface. This embodiment can become advantageous such

5 as where a substrate is involved having a relatively greater  
surface roughness and it is necessary to account for any  
10 discontinuities in the surface profile by sufficiently  
building-up the diffusion layer to blanket the surface  
5 topography presented and provide complete coverage. To build-up  
multiple monolayers, one stacked upon the other, MBE deposition  
15 can be used to sequentially deposit additional monolayers of  
metal atoms using an elemental source of the metal. In this  
20 way, a diffusion barrier film thickness can be assembled up to  
10 any desired thickness, but preferably is maintained at or below  
not more than 100 Å, more preferably not more than 20 Å to  
25 meet the primary objective of providing an extremely thin yet  
effective diffusion barrier.

As can be appreciated, a semiconductor device is obtained  
30 15 by this invention in which a monolayer or several monolayers of  
metal atoms separates a metallic conductor from other materials  
in the device, such as semiconductor or insulating materials,  
35 in which the extremely thin diffusion barrier film serves as an  
effective barrier preventing atoms of the metallic conductor  
20 from diffusing into such other materials and either impairing  
40 the device or rendering it totally inoperative.

Various other objects, details and advantages of the  
invention will be apparent from the following detailed  
45 description when read in conjunction with the drawings.

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**Brief Description of Drawings**

FIG. 1 is a schematic cross-section depicting diffusion of copper into a silicon substrate, where no diffusion barrier is present;

FIG. 2 is a graph illustrating the projected requirement in diffusion barrier thickness by the Semiconductor Industry Association;

FIG. 3 is a schematic cross-section depicting the effect of a diffusion barrier in accordance with the invention;

FIG. 4 is a schematic diagram illustrating the process of deposition of a diffusion barrier precursor compound, and a metallization layer, onto a substrate by molecular beam epitaxy;

FIGS. 5A-E is a schematical illustration showing the interfacial structure of the diffusion barrier on an atomic level as it is being formed on a semiconductor substrate after various process steps according to an inventive process;

FIG. 6 is a schematic diagram illustrating the process of deposition of a diffusion barrier precursor compound onto a substrate by r.f. sputtering; and

FIG. 7A is a schematical illustration showing the interfacial structure of the barrier film on an atomic level where the barrier film is comprised of a plurality of contiguous monolayers, while FIG. 7B shows another embodiment of the invention where the barrier film is a composite monolayer formed of different types of metal atoms, and FIG. 7C shows yet another embodiment where the barrier film is

5 comprised of a plurality of contiguous monolayers in which  
different monolayers thereof are formed of different types of  
10 metal atoms.

FIG. 8 is a schematic cross-sectional view showing a  
5 diffusion barrier in accordance with the invention preventing  
diffusion of a copper plug into silicon substrate and into a  
15 silicon dioxide insulating layer overlying the substrate.

#### 20 Best Mode for Carrying Out the Invention

10 FIG. 1 illustrates a typical attempt at copper  
metallization of a silicon semiconductor substrate 10. The  
25 substrate, which is made up of silicon atoms 12, has two  
laterally delineated copper interconnect strips 14 deposited on  
its surface. In the annealing process, copper atoms 16 tend to  
30 15 diffuse into the substrate, impairing its semiconducting  
properties, and usually rendering it totally inoperative, by  
effectively creating an electrical short circuit. Similar  
35 diffusion occurs at an interface between a copper conductor and  
a SiO<sub>2</sub> insulating layer, for example in the case in which an  
20 attempt is made to deposit a conducting copper plug in a via  
40 hole in the SiO<sub>2</sub> insulating layer. Diffusion of copper atoms  
into the SiO<sub>2</sub> insulating layer impairs its effectiveness as an  
insulator and may have a serious adverse effect on the  
45 properties of the device.

25 As mentioned above, various attempts have been made to  
achieve a diffusion barrier to permit the use of copper  
50 conductors in semiconductor devices. The most attention so far

5 has been given to the use of nitrides of tungsten and titanium.  
Various other diffusion barrier materials, for example tantalum  
10 nitride, have also been tried. As shown in FIG. 2, which is  
based on published Semiconductor Industry Association data,  
5 presently achievable diffusion barrier thicknesses are only in  
15 the 200-250 Å range for tantalum nitride, although thicknesses  
smaller than that are expected to be pursued by the industry in  
the upcoming years.

20 This invention provides an effective diffusion barrier  
10 having a thickness well below 100 Å, and below 5 Å in one  
exemplary embodiment, which is far below the minimum thickness  
25 projected by the industry data depicted in FIG. 2. The  
extremely thin diffusion barrier layers achievable by this  
invention potentially could be useable long after alternative  
30 15 technologies become obsolete.

Referring now to FIG. 3, a portion of an integrated  
circuit is schematically illustrated on an atomic level that  
35 comprises a silicon substrate 18 made up of silicon atoms 20,  
and having laterally delineated copper interconnect strips 22.  
20 At the upper surface of the silicon substrate 18, a monolayer  
40 of barium (Ba) atoms 24 is interposed between the conductor  
strips 22 and the surface of the substrate 18 and effectively  
prevents diffusion of the copper atoms into the silicon. The  
45 layer of Ba atoms need only have a thickness of one atomic  
25 layer, i.e., a monolayer of approximately  $5 \times 10^{-10}$  meters (5Å)  
in thickness, in order to provide the desired barrier to  
50 diffusion of the conductor into the adjoining substrate. The

5 barium layer depicted in Fig. 3 illustrates the situation in  
which a single monolayer of barium is provided. The extremely  
10 small thickness of the diffusion barrier contributes to the  
reduction in both thickness and the lateral dimensions of the  
5 integrated circuit layer, and the ability to use copper  
interconnects and other conductor materials otherwise  
15 predisposed to creating diffusion problems (e.g., Au, Ag, Pt)  
instead of aluminum interconnects. As such, the present  
invention represents a remarkable breakthrough in the field.

10 As will become apparent from the following description, in  
one mode of this invention, a diffusion barrier comprised of  
metal atoms and having a thickness of not more than  
25 approximately 5Å is achievable by depositing a metal halide  
precursor compound on a semiconductor or insulating substrate  
so as to form a temporary heteroepitaxial film thereon. Then,  
30 the resulting temporary heteroepitaxial film created by the  
metal halide and the substrate surface is subjected to a post-  
growth anneal or chemical etching in which all of the temporary  
35 heteroepitaxial film is eliminated by removal from the  
substrate except for an atomic layer of the metal component,  
40 i.e., a monolayer. This residual monolayer of metal atoms  
disposed in contact with the substrate surface provides a  
diffusion barrier to conductor materials.

45 One suitable approach for depositing the metal halide used  
25 as a precursor compound for forming the diffusion barrier layer  
is molecular beam epitaxy (MBE), such as depicted in FIG. 4. A  
50 substrate 26, e.g., a silicon wafer, is supported on a rotating

5 holder 28 within a conventional MBE deposition chamber 30. The  
deposition chamber is illustrated in simplified form. Not  
10 shown are provisions for raising the temperature of the  
substrate to annealing temperatures and for evacuating the  
5 chamber. Also not shown is a conventional Reflective High  
15 Energy Electron Diffraction (RHEED) diagnostic system directed  
toward the substrate 26.

A diffusion barrier precursor compound effusion cell, for  
20 example a barium fluoride, strontium fluoride or the like  
effusion cell, is provided at 32, and has a shutter 33. A  
10 shutter 35 is also provided for the silicon wafer 26. An  
25 electron beam source for the metallization layer, e.g., copper,  
is shown at 34.

In the operation of the MBE deposition apparatus of FIG.  
30 4, the substrate 26 is placed inside the chamber 30 and  
positioned by rotatable holder 28 and the chamber 30 is  
evacuated, using ion pumps and liquid nitrogen trapping to  
35 achieve a high vacuum. The substrate 26 is vacuum annealed to  
remove any passivation layer by deoxidation, for example  
20 silicon dioxide in the case of a silicon wafer.

40 The temperature of the substrate 26 is then reduced to a  
suitable deposition temperature, and the effusion cell 32 is  
heated while the substrate 26 is mechanically rotated. The  
45 electron beam of a RHEED diagnostic system is focused onto the  
substrate 26 and the RHEED pattern is monitored. When the  
25 RHEED pattern corresponding to the single crystal substrate  
surface appears (indicating complete removal of the passivation  
50

5 layer) on the RHEED screen, the shutters 35 and 33 in front of  
the substrate holder 28 and the effusion cell 32, respectively,  
10 are opened to allow precursor molecules to impinge on the  
substrate surface 29. Deposition of the precursor 27 onto the  
5 silicon surface 29 begins, and is allowed to continue until the  
single crystal silicon RHEED pattern disappears and is replaced  
15 by a pattern corresponding to a single crystal layer of the  
precursor compound. Deposition is halted by closing the  
substrate and effusion source shutters 35 and 33, respectively.  
20 By this juncture, a temporary heteroepitaxial film derived from  
the precursor molecules is situated on the substrate surface  
25 29, although the nature of the interface is more complicated as  
will become apparent from later descriptions herein.

During the deposition of the precursor 27 on the substrate  
30 26, the substrate 26 should be at a temperature in the range  
15 from approximately 500°C to 800°C, and ideally at approximately  
750°C, though the temperature will vary depending on the  
35 particular substrate and the processing tool. The pressure  
within the deposition chamber 30 should be  $10^{-8}$  mbar or less,  
20 more preferably  $10^{-9}$  mbar or less, and still more preferably  
40  $10^{-10}$  mbar or less, in the case of depositing a metal halide on  
a silicon substrate. The time required to achieve adequate  
45 deposition of the precursor sufficient to form the temporary  
heteroepitaxial film on the substrate is typically one or two  
25 minutes, but is not limited thereto.

50 Following the deposition on the substrate of the temporary  
heteroepitaxial film derived from the precursor compound, the

5 temperature of the substrate is raised to cause precursor  
molecules to detach from the temporary heteroepitaxial film on  
10 the substrate. In the case of  $\text{BaF}_2$ , barium atoms adjacent to  
the substrate remain tightly adhered thereto as a two-  
5 dimensional monolayer, while fluorine atoms (as bonded to other  
barium atoms) in the temporary heteroepitaxial film are  
15 effectively re-evaporated in the form of barium fluoride and  
eliminated from the temporary heteroepitaxial film. This will  
cause the RHEED pattern to change in appearance. Specifically,  
20 the "reappearance" of a RHEED pattern similar to that for the  
single crystal substrate confirms that the precursor molecules  
have been evaporated. The substrate temperature at which the  
detachment of the precursor molecules with the halogen atoms  
from the temporary heteroepitaxial film takes place during the  
30 15 post-growth anneal step is not necessarily limited, but should  
be in the vicinity of 750°C to 1000°C, preferably 800°C. The  
monolayer of metal atoms which remains on the substrate serves  
as the diffusion barrier between the substrate and any  
35 metallization layer subsequently deposited upon it. The  
20 metallization layer can be deposited by any of various standard  
40 microelectronic metallization methods, and, in this embodiment,  
it can be conveniently deposited while the substrate is still  
in the MBE chamber by operation of the electron beam source.

45 The crystallographic and chemical characterization of the  
25 aforesaid temporary heteroepitaxial film, and the effect of  
treatments thereof according to this invention to form a  
50 diffusion barrier film on the substrate, are now discussed in

5 greater detail. Based on X-ray photoelectron spectroscopy (XPS)  
and heavy ion backscattering spectroscopy (HIBS) analyses of  
10 the precursor compound/substrate surface interfacial chemistry,  
the formation of an ultra-thin metal monoatomic layer  
5 (monolayer) on the substrate is considered to proceed by a  
multi-stage process, which is schematically illustrated in  
15 FIGs. 5A-E. XPS and HIBS analysis measurements referred to  
herein can be performed using generally available equipment and  
20 analyses protocol understood and implementable by one skilled  
10 in the art.

As schematically illustrated in FIG. 5A,  $\text{BaF}_2$  molecules 50  
25 are directed and impinged onto the surface 51 of a silicon  
substrate 52, such as by MBE deposition. For FIGs. 5A-E,  $\text{BaF}_2$   
is used to illustrate the metal halide, and silicon is used to  
30 15 illustrate the (semiconductor) substrate, although other  
materials can be used as indicated elsewhere herein.

Ideally, the silicon surface 51 to be used as the  
35 deposition substrate has a highly planar, smooth surface to  
minimize the coating thickness needed to provide complete  
20 coverage thereof. Decoxidation annealing, chemical-mechanical-  
40 planarization (CMP) polishing or ion milling can be used in a  
pretreatment of the silicon surface prior to deposition of the  
diffusion barrier to enhance the planarity and smoothness of  
45 silicon surface, if necessary. On the other hand, as will be  
25 described below, the inventive process itself provides some  
measure of in situ planarization of the silicon surface during  
50 MBE deposition.

5 In any event, in the first step, the  $BaF_2$  molecules react with silicon atoms 51a, 51b, 51c, and so forth, at the surface 51 of the silicon substrate 52. The Ba-F and silicon-silicon bonds at the surface of the silicon substrate are broken. As 10 schematically shown in FIG. 5B, the free silicon and fluorine atoms at the vicinity of the interface where the barium fluoride molecules are contacting the silicon surface 51 then 15 combine to form volatile silicon-fluoride compounds ( $SiF_4$ ) 53 which escapes from the silicon substrate surface 51, and it is 20 extracted from the MBE chamber via vacuum. Although FIG. 5B depicts compound 53 as two halide atoms (white circles) bonded to a common metal atom (darkened circle), it will be understood that this illustrative only because other gaseous metal-halides may be generated, such as tetrahalides of silicon where the 30 substrate 52 is silicon. By comparison, if the substrate 52 instead is GaAs, the escaping gas 53 would be GaF. This etching-like effect upon the surface silicon atoms serves to 35 effectively smoothen the silicon surface. In any event, as illustrated in FIG. 5B, the barium atoms left behind bond with 20 dangling bonds of the surface silicon atoms, forming a 40 monoatomic layer 54 of metal atoms, i.e., a metal monolayer of barium atoms. This deposition step proceeds for a sufficient duration of time to form a continuous layer of barium atoms 45 across the surface of the silicon substrate without leaving any 25 bare spots.

50 As illustrated in FIG. 5C, once complete coverage of the silicon substrate 52 with barium atoms 54 is achieved, barium

5 fluoride 50 deposition via MBE is continued from a molecular  
beam. As illustrated in FIG. 5D, this subsequently introduced  
10 barium fluoride adheres to the barium monolayer 54 and grows  
epitaxially thereon to form a temporary homoepitaxial film  
5 portion 55. The amount of subsequent deposition of epitaxial  
barium fluoride on the barium monolayer is allowed to be enough  
15 to provide a safety measure which ensures complete substrate  
coverage with a monolayer of barium atoms. In this way a  
heteroepitaxial film 56 is formed on the substrate surface 51  
20 comprising a monolayer 54 of metal (e.g., Ba) atoms as an  
interaction regime attached directly to the substrate surface  
51 and a homoepitaxial regime 55 comprised of oriented  
25 molecular metal halide (e.g., barium fluoride) formed, in turn,  
on the monolayer 54. The homoepitaxial regime 55 of  $BaF_2$  of the  
temporary heteroepitaxial film 56 is (100)-oriented on silicon  
30 (100), and (111)-oriented when the substrate is silicon (111),  
GaAs (100), or GaAs (111).

35 XPS measurements have confirmed that barium atoms have the  
two above-mentioned different chemical states, i.e., the  
20 interaction (metal monolayer) and the homoepitaxial regimes, in  
the temporary film present at this stage of processing. The  
40 relative abundance of these two states has also been determined  
by XPS. The number of barium atoms in each state is  
45 determinable by normalizing integrated XPS peak intensities to  
HIBS measurements of the total number of barium atoms on the  
25 surface. The results of these analyses confirm that  $BaF_2$  first  
50 reacts with the silicon surface during initial MBE deposition.

5 at the silicon surface and dissociates, releasing a gaseous  
silicon-fluorine compound. This reaction is self-limiting,  
10 resulting in a barium monolayer that enables subsequent  $\text{BaF}_2$   
molecules to form an epitaxial (111)-oriented film on the  
5 silicon surface. Then, a post-growth anneal affects evaporation  
15 of the barium fluoride deposited on the monolayer.

That is, as illustrated in FIG. 5E, in a second stage of  
this inventive procedure, which is conducted after the MBE  
20 deposition of the metal halides on a substrate to form the  
10 temporary heteroepitaxial film 56 shown in FIG. 5D,  
a vacuum anneal is performed to cause evaporation of barium  
25 fluoride 57 from the temporary heteroepitaxial film such that  
the barium fluoride content found in the homoepitaxial portion  
thereof (feature 55 in FIG. 5D) is completely removed back to  
30 15 the monolayer 54 of barium atoms attached to the silicon  
surface 51. Alternatively, the homoepitaxial portion 55 of the  
temporary heteroepitaxial film can be removed by etching (e.g.,  
35 chemical etching) which is selective between the homoepitaxial  
portion 55 and the monolayer portion 54 such that the former  
20 can be removed while leaving the latter intact.

40 In any event, prior to performing the post-growth anneal  
(or etching) to remove the homoepitaxial portion 55 of the  
temporary heteroepitaxial film, there is no practical limit on  
45 how thick the overdeposit of barium fluoride can be that is  
25 formed over the barium monolayer. However, it will be  
appreciated that the thicker the deposited barium fluoride  
50 layer(s) of the homoepitaxial portion of the temporary film is

5 made to be, the longer the post-growth anneal time that will be  
necessary to decompose the deposited thickness of barium  
10 fluoride molecules back to the monolayer of barium atoms left  
attached to the substrate surface.

5 The MBE deposition of the temporary heteroepitaxial film  
and the post-growth anneal can be performed in the same  
15 processing chamber without breaking the vacuum between the two  
procedures. Alternatively, the MBE deposition can be performed  
20 in a first processing tool, after which the vacuum is broken,  
10 and the workpiece is then transferred to another processing  
tool for separately performing the post-growth anneal at which  
25 time the substrate is heated up again with a vacuum being  
created in the second processing tool. In the latter case, the  
heteroepitaxial portion of the temporary heteroepitaxial film  
30 15 serves as a protective coating over the monolayer portion of  
the heteroepitaxial film during such transit between separate  
processing tools.

35 In that the atomic diameter of barium is 4.48 Å, and that  
of strontium is 4.29 Å, it can be appreciated how the  
20 formation of a monolayer of these metal atoms, for example, on  
40 a substrate by the techniques presented herein permits the  
formation of an extremely thin, yet effective diffusion  
barrier.

45 While not desiring to be bound to any particular theory,  
25 it nonetheless is thought that the underlying mechanism by  
which the metal monolayer prevents diffusion of the copper, or  
50 other highly diffusive metal, through the barrier layer into

5 the semiconductor or insulating substrate is at least in part  
attributable to the fact that metal atoms are provided in the  
10 monolayer which have relatively large electron clouds which can  
overlap or touch each other between the metal atoms to  
5 effectively form an energy barrier against movement of copper  
atoms therethrough. As will be understood by one of ordinary  
15 skill in the art, from a standpoint of terminology, the  
electron clouds are also spoken of as atomic orbitals occupied  
by electrons in different energy levels or shells, and the  
20 electron cloud is a cloud of negative charge formed of  
electrons of an electron density distribution corresponding to  
25 the element at issue.

An important advantage of the invention is the ease with  
which the diffusion barrier layer can be formed. Where metal  
30 halides are used as a precursor in forming the diffusion  
barrier film, the precursor, e.g.,  $\text{BaF}_2$  or  $\text{SrF}_2$ , can be  
deposited for a sufficient duration of time to ensure complete  
35 coverage of the silicon substrate. Such complete coverage can  
be achieved within relatively short period of time, e.g., about  
20 one minute using MBE deposition of a metal halide on the  
40 substrate, depending on deposition conditions. Also, the  
length of deposition time is not critical provided it is at  
least high enough to establish the diffusion barrier film;  
45 deposition times of several minutes are not detrimental to the  
25 procedure, and the deposition temperature also is not critical.  
In the second step, all components of the precursor except for  
50 the monolayer of metal atoms, are removed by the post-growth

5 annealing procedure. The metal atoms of this thin layer adhere  
tightly to the substrate, and consequently, the second step can  
10 be carried out over a wide range of time and temperature  
conditions without adversely affecting the formation and  
5 character of the diffusion barrier layer.

15 By way of a specific illustration of forming a diffusion  
barrier on a semiconductor substrate,  $\text{BaF}_2$  can be used as the  
barrier film precursor and a silicon wafer can be used as the  
20 substrate. The silicon substrate first is deoxidized by vacuum  
annealing at  $900^\circ\text{C}$  for one hour to remove the silicon dioxide  
10 passivation layer. Then the substrate can be brought to a  
deposition temperature of  $750^\circ\text{C}$  in a VG Semicon V80H MBE growth  
25 chamber at a vacuum of less than  $1 \times 10^{-10}$  mbar. All temperature  
measurements are made from a noncontact thermocouple gauge. A  
30  $\text{BaF}_2$  effusion cell can be heated to  $1050^\circ\text{C}$ . While the  
substrate holder is mechanically rotated, an electron beam from  
a RHEED diagnostic system is directed toward the substrate.  
35 The beam is focused until the RHEED pattern of a single crystal  
silicon surface appears on the RHEED screen. The shutters in  
20 front of the substrate holder and the effusion cell are then  
40 opened to allow  $\text{BaF}_2$  molecules to impinge on the substrate  
surface. Deposition of  $\text{BaF}_2$  is allowed to continue until the  
single crystal silicon RHEED pattern disappeared and is  
45 replaced by a single crystal  $\text{BaF}_2$  pattern. Deposition is then  
25 halted by closing the substrate and effusion source shutters.  
The substrate temperature is then raised to  $800^\circ\text{C}$  and held  
50 until a RHEED pattern similar to that of the single crystal

5 silicon substrate reappears. It will be understood that the  
above-provided exemplary protocol is provided merely for sake  
10 of illustration, and not limitation.

In the mode of the invention being discussed above in  
5 which metal halides are used as precursor compound for forming  
the diffusion barrier film, the precursor compounds that can be  
15 used include, for example,  $\text{BaF}_2$ ,  $\text{BaCl}_2$ ,  $\text{SrF}_2$ ,  $\text{SrCl}_2$ ,  $\text{CsF}$ ,  $\text{CsCl}$ ,  
 $\text{RbF}$ , and  $\text{RbCl}$ , and the like. Especially preferred are those  
20 metal halide salts that have cubic halide, e.g. a cubic  
fluorite, crystal structure. While not desiring to be limited  
10 to any particular theory at this point, applicants nonetheless  
consider that precursor compounds obtainable as metal halides,  
25 e.g.,  $\text{BaF}_2$ ,  $\text{BaCl}_2$ ,  $\text{SrF}_2$ ,  $\text{SrCl}_2$ ,  $\text{CsF}$ ,  $\text{CsCl}$ ,  $\text{RbF}$ , and  $\text{RbCl}$ , and  
the like, that have cubic crystal structure will tend to  
30 provide sources of metal atoms that are amenable to the above-  
discussed decomposition reaction and interaction with the  
silicon surface under readily implementable MBE and annealing  
35 processing conditions. Although not desiring to categorically  
exclude all metal halide salts having rutile crystal structure,  
20 rutile metal halide salts may not be suitable for many  
processing environments as they do not normally decompose under  
40 typical MBE conditions.

In another mode of the invention for forming the diffusion  
45 barrier film, the monolayer of metal atoms alternatively can be  
25 formed in a one step operation (i.e., without a post-growth  
anneal step) by directly depositing an elemental form of the  
50 metal atoms, such as barium, via MBE on the surface of the

5 semiconductor substrate. Since certain elemental metals such as  
barium are highly reactive, appropriate precautions have to be  
10 taken to handle, maintain and process the elemental barium in  
an inert environment, e.g., under an argon gas atmosphere, up  
5 until it is deposited upon the semiconductor.

15 Also, in another embodiment of this invention, it is  
possible to form the monolayer of metal atoms directly on the  
semiconductor substrate by the above-described two-step  
20 decomposition reaction process involving a metal halide (i.e.,  
MBE deposit/post-growth anneal), and then to increase the  
10 thickness of the diffusion barrier film by depositing one or  
more additional monolayers of metal atoms on the original  
25 monolayer through depositing the elemental form of the metal  
atoms, such as barium, via MBE on the original monolayer. That  
30 is, while formation of a single monolayer on the substrate as  
described above is sufficient to meet the diffusion barrier  
objectives of this invention, it is also within the scope of  
35 this invention to form one or more additional monolayers of the  
metal on the original monolayer as long as the overarching  
20 objective of forming a diffusion layer of extremely small  
40 thickness is maintained. For example, the metal atom can be  
deposited from an elemental form via MBE on the surface of the  
silicon substrate. In this way, a plurality of monolayers can  
45 be formed as contiguous layers upon the substrate to form an  
25 overall thickness in the diffusion barrier layer of any desired  
thickness. Since thin thicknesses are desired, the diffusion  
50 barrier preferably is built up to an overall thickness that

5 does not exceed  $100\text{\AA}$ , and more preferably does not exceed  $20\text{\AA}$ .  
FIG. 7A illustrates this scenario in which a plurality of  
10 monolayers 71a, 71b, and 71c are sequentially formed, upon the  
surface 72 of substrate 73, one on the other, in the manners  
5 described above. Then, a conductor material or other material  
(not shown) can be formed over the outermost monolayer 71c. In  
15 this embodiment, each of monolayers 71a, 71b, and 71c are  
formed of the same type of metal atoms, and together, they form  
the barrier film. Also, while three monolayers are depicted in  
20 FIG. 7A, the plurality of monolayers can be two or more.

Also, it is possible to deposit a combination of different  
25 types of metal atoms during precursor deposition on a substrate  
to form a composite diffusion barrier monolayer. For example,  
because the melting and sublimation temperatures of strontium  
30 fluoride and barium fluoride are similar, the temperature  
ranges for MBE deposition of a strontium fluoride precursor  
onto silicon and for the evaporation of the strontium fluoride  
35 precursor from silicon almost completely overlap those given  
above for barium fluoride. Thus, temperatures in the mid-  
20 portion of the ranges given for barium fluoride on silicon are  
40 also satisfactory for the MBE deposition and evaporation of  
strontium fluoride. However, the temperatures required to  
45 sublimate, i.e., directly change the state of the source solid  
crystal form to a gas for deposition via MBE, for barium  
25 fluoride and strontium fluoride are slightly different.  
Consequently, to control the ratio of barium to strontium in a  
50 composite monolayer of a barrier layer to be formed, the barium

5 fluoride and strontium fluoride should be deposited using  
separate effusion cells for the MBE chamber. In any event, a  
10 composite monolayer can be formed of barium and strontium atoms  
in this manner. FIG. 7B illustrates this embodiment of the  
5 invention where the barrier film is a composite monolayer 71  
formed of different types of metal atoms 71d and 71e. Two or  
15 more different types of metal atoms can be provided in the  
composite monolayer 71. Then, a conductor material or other  
20 material (not shown) can be formed over the composite monolayer  
10 71.

Also, if an additional monolayer or monolayers are  
25 deposited on the original monolayer formed on the surface of  
the substrate, the different monolayers can have the same or  
different types of metal atoms by appropriate selection of the  
30 15 precursor compounds at the different stages of processing. For  
instance, as illustrated in FIG. 7C, the barrier film is  
comprised of a plurality of contiguous monolayers 71f, 71g and  
35 71h in which different monolayers thereof are formed of  
different types of metal atoms. In this illustration, layers  
20 71f and 71h are formed of the same type of metal atoms while  
40 intervening monolayer 71g is formed of a metal atom that is  
different from the metal atoms in layers 71f and 71h. However,  
45 there is no requirement that barrier film arrangements with  
three or more monolayers containing the different types of  
25 metal atoms must alternate through the stack of monolayers in  
any particular pattern. Also, while three monolayers are  
50 depicted in FIG. 7C, the embodiment is not limited to that

5 plural number. Also, composite monolayers, such as described in  
FIG. 7B can be used in combination with one or more contiguous  
10 monolayers formed thereon having a single type of metal atoms,  
such as shown in FIG. 7A, or different types of metal atoms in  
5 different respective monolayers, such as illustrated in FIG.  
15 7C.

As yet another mode of applying the metal halide precursor  
to the substrate to form the temporary heteroepitaxial film,  
20 r.f. sputtering, such as depicted in FIG. 6, can be used. In a  
10 sputtering chamber 36, an argon-ion gun 38 directs a beam 40  
onto a supply (target) 42 of barium fluoride, for example,  
25 causing deposition of barium fluoride onto a substrate 44 by  
sputtering. Here, as in the case of MBE deposition, the post-  
growth annealing of the substrate can take place within the  
30 15 sputtering chamber in order to remove  $BaF_2$  molecules and the  
fluorine atoms leaving only a thin layer of barium atoms as a  
monolayer adhering to the surface of the substrate. The  
35 metallization (conductor) layer can also be applied to the  
substrate while it is inside the sputtering chamber.  
20 Sputtering can also be used to deposit a diffusion barrier of  
40 other metal atoms, such as strontium atoms, in a similar  
manner. Also, a combination of different types of metal atoms  
45 could be sputtered in the same monolayer or in different  
monolayers using different sputtering targets formed of  
25 different respective metal halide precursors. In general,  
50 however, MBE is superior to r.f. sputtering because sputtering  
can cause dissociation of the barium-fluorine bond before the

5 barium fluoride molecule reaches the substrate surface which facilitates the formation of the temporary heteroepitaxial film.

10 As other different modes for forming the diffusion barrier film on a substrate, deposition processes other than MBE and r.f. sputtering can be used, for example, physical and chemical vapor deposition, wet chemical processes, and liquid phase epitaxy. For instance, precursors used in metal-organic chemical vapor deposition (MOCVD) to form the diffusion barrier 15 on a semiconductor or insulating substrate include Ba (2,2,6,6-tetramethyl-3,5 heptanedionate) and Sr (2,4-pentanedionate).

25 As illustrated in FIG. 8, the diffusion barrier produced in accordance with the invention can be used not only to prevent diffusion of conductor metals into a semiconductor substrate, but also to prevent diffusion of the conductor metal 30 into an insulating layer. In FIG. 8, layer 46 is a semiconductor substrate, for example, a semiconducting layer of silicon, and layer 48, which overlies layer 46, is an insulating layer of silicon dioxide ( $\text{SiO}_2$ ). A plug 45 of a metal, such as copper, is located in a via hole through 35 insulating layer 48, and makes ohmic contact with the semiconducting layer 46 through a thin diffusion barrier layer 49 of barium formed by one of the processes described above. This plug is used to conduct current between layer 46 and 40 another layer (not shown) which is separated from layer 46 by insulating layer 48. In the same process, the sidewall of the via hole is lined with a barium diffusion barrier 49, which 45 50

5 prevents diffusion of the copper into the insulating layer.  
The barium or strontium atoms are deposited onto an insulating  
layer in the same way in which they are deposited onto silicon.

10 As will be apparent from FIG. 8, the minimization of the  
5 thickness of the side wall diffusion barrier 49 makes it  
possible to use copper for interconnections between layers.  
15 The copper interconnects can be significantly narrower than  
tungsten interconnects having the same current capacity, and  
the diffusion barrier is also very thin. Therefore the use of  
20 the diffusion barrier in accordance with the invention as a  
liner for via holes in insulating layers, can contribute  
25 significantly to the minimization of the lateral dimensions of  
an integrated circuit of which the elements shown in FIG. 8 are  
a part. Because the diffusion barrier 49 is very thin, it  
30 15 permits the use of via holes of relatively low aspect ratio,  
making them easier to fill with conducting metal and  
eliminating voids which result in failures or rejection of ICs.

35 It will be understood that this invention is not limited  
to the above illustrated substrate materials, conductor  
20 materials, and materials used to make the diffusion barrier, as  
40 long as other criterion understood and set forth herein for  
these respective materials are satisfied.

45 For instance, the material used for forming the diffusion  
barrier can be any appropriate metal in elemental form or  
25 precursor molecular compound from which a layer of metal atoms  
(i.e., a monolayer) can be formed on a semiconductor or  
50 insulating substrate.

5           The substrate material upon which the diffusion barrier is  
formed is not particularly limited and can include  
10 semiconductor materials and insulating materials used in  
semiconductor device fabrications. The semiconductor material  
5 can be, for example, Si, Ge, InP, GaAs, SiC, GaN, AlN, InSb,  
15 PbTe, CdTe, HgTe, Hg<sub>1-x</sub>Cd<sub>x</sub>Te, PbSe, PbS, and tertiary  
combinations of these materials. The semiconductor material can  
be monocrystalline or polycrystalline. The semiconductor  
20 substrate can be in bulk wafer form, deposited or grown layer  
10 form (e.g., epitaxially grown), or silicon-on-insulator (SOI)  
form. The semiconductor can be doped or undoped with impurities  
25 (e.g., p-, n-doping). The insulating substrate material can be,  
for example, SiO<sub>x</sub>, SiO<sub>2</sub>, BaF<sub>2</sub>, SrF<sub>2</sub>, CaF<sub>2</sub>, silicon nitride, PSG,  
or BPSG. For example, a thin diffusion barrier film formed of  
30 15 a barium, strontium or cesium monolayer (or monolayers) can be  
used to line via holes in insulators made of BaF<sub>2</sub>, SrF<sub>2</sub>, and  
CaF<sub>2</sub>.

35           As to the types of conductor materials that can be formed  
on the diffusion barrier, these include conventional metals and  
20 metal alloys used for wiring line, interconnects, bonding pads,  
40 and so forth, in semiconductor device or opto-electronic device  
fabrication. The present invention is especially useful for  
providing an in situ barrier to electrically conductive metals  
45 which tend to diffuse into semiconductor and insulating  
25 materials common to semiconductor processing. These conductive  
metals include, for example, pure copper, copper alloys (e.g.,  
50 Cu-Al, Cu-Si-Al), copper doped with a dopant (e.g., aluminum)

5 that impedes electromigration, gold, silver, or platinum. In  
the case of copper, it may be desirable to alloy it with small  
10 percentages (e.g., < 5%) of other metallic substances to  
prevent electromigration. The conductor material can be  
5 deposited on the diffusion barrier by any conventional  
technique, including, e.g., electroplating, electroless  
15 deposition, sputtering, chemical vapor deposition, e-beam  
evaporation, and so forth. For example, copper can be deposited  
20 by e-beam evaporation at  $1 \times 10^{-9}$  millibars in a heated chamber,  
10 or at  $10 \times 10^{-11}$  millibars under a nitrogen environment. The  
conductor film can be patterned on the diffusion barrier by  
25 various techniques, such as by conventional additive or  
subtractive processes known and used in semiconductor  
processing (e.g., photolithographic processing). The invention  
30 15 can also be used to prevent diffusion of gallium and/or arsenic  
from gallium arsenide into silicon and other substrates.

35 A number of advantages and improvements are achieved by  
the present invention which can be exploited in the  
semiconductor device processing industry. A principal advantage  
20 of this invention is that the thickness of the diffusion  
40 barrier layer can be made extremely thin. In practice,  
depending on the surface characteristics of the substrate  
material onto which the diffusion barrier layer is deposited,  
45 the thickness of the diffusion barrier layer according to this  
25 invention will generally be formed in the range of  
approximately 5 Å to 100 Å. In the case of a smooth, highly  
50 planarized substrate material, e.g., a substrate having a

5 surface roughness well below 5Å, the diffusion barrier can be  
made as thin as one monolayer, which will have a thickness  
10 slightly less than 5 Å corresponding the atomic diameter of  
the metal atoms forming the diffusion barrier. For such smooth  
5 substrates, the diffusion barrier formed of one monolayer  
having a thickness less than 5Å in thickness will  
15 satisfactorily inhibit diffusion of copper and other conductors  
into the substrate. With substrate materials having a  
relatively greater surface roughness, the thickness of the  
20 diffusion barrier layer will tend to vary. For instance, the  
diffusion barrier layer on a substrate having a surface  
25 roughness greater than 5Å may be formed so as to have a  
thickness value in the range of approximately 5 to 100 Å, with  
metal atoms of the diffusion barrier layer accumulating at any  
30 15 step edges on the substrate surface. Thus, the diffusion  
barrier film of this invention is only one monolayer or a  
multiple number of contiguous monolayers formed on the  
35 substrate surface, and in any event, it need not be more than  
approximately 100Å in total thickness to achieve the objectives  
20 of this invention for current and future anticipated  
40 semiconductor device fabrication specifications. A large scale  
integrated circuit having copper conductors and a diffusion  
45 barrier film according to this invention with a thickness in  
the range of approximately 5Å to approximately 100Å, can  
25 achieve an extremely high component density, which reduces the  
number of layers required for a given number of components, and  
50 very low heat dissipation. In the practice of this invention.

5 therefore, the diffusion barrier thickness can vary from a  
thickness less than about 5Å to a greater thickness, which can  
be up to about 100Å, preferably up to no more than 20Å.

10 Conventional alternative diffusion barriers are significantly  
5 thicker than 100Å.

15 Another advantage of the invention is that the diffusion  
barrier film, where it is barium or strontium, or a similar  
metal, is compliant, i.e., it is mechanically soft and easily  
20 deformable. The compliance of the diffusion barrier film allows  
10 dissimilar materials to be put together without introducing  
defects, such as voids or mechanical stresses, at the interface  
25 which may have detrimental effects on device performance, the  
diffusion barrier film, or the metallization layer.

Furthermore, barium and strontium, or like metals, can form  
30 15 intermetallic compounds with copper ( $\text{BaCu}_{11}$  and  $\text{Cu}_5\text{Sr}$  are  
examples), causing copper atoms to be tightly bound to the  
barium or strontium at the interface and unable to migrate past  
35 the barium or strontium layer into the silicon.

Also, while the barrier film based on one or more  
20 monolayers of metal atoms that is used in this invention has  
40 been illustrated herein specifically as a barrier to diffusion  
of metal conductors into substrate materials, it will be  
understood that the barrier film is not necessarily limited to  
45 that use alone, as it possesses many advantageous attributes  
25 that could be exploited in semiconductor device fabrications.  
For example, the barrier film could be used as a barrier layer  
50 in the fabrication of semiconductor laser devices, such as

5 those having heterojunctions and incorporating different  
semiconductor materials, e.g., GaAs on top of silicon.

10 While the invention has been shown and described with  
reference to certain preferred embodiments, it will be  
5 understood by those skilled in the art that changes in form and  
detail may be made without departing from the spirit and scope  
15 of the appended claims.

## Claims

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Claims

1. A semiconductor device, comprising:

a substrate (18), a barrier film (24) on the substrate (18), a material (22) directly on the barrier film (24);

characterized in that the barrier film (24) includes a monolayer on the substrate (18).

2. A semiconductor device according to claim 1, wherein the barrier film (24) has a thickness less than 100Å.

3. A semiconductor device according to claim 1, wherein the barrier film (24) has a thickness less than 20Å.

4. A semiconductor device according to claim 1, wherein the monolayer of the barrier film (24) comprises metal atoms selected from barium atoms, strontium atoms, cesium atoms, and rubidium atoms, singly or in combinations thereof, located on said surface of said substrate (18).

5. A semiconductor device according to claim 1, wherein the barrier film (24) comprises a plurality contiguous monolayers (11a-c) of metal atoms located on the surface of the substrate material (18).

6. A semiconductor device according to claim 1, wherein the barrier film (24) comprises a plurality of contiguous monolayers comprising two or more different types of metal

5 atoms selected from the group consisting of barium atoms,  
strontium atoms, cesium atoms, and rubidium atoms, located on  
10 said surface of said substrate (18).

5 7. A semiconductor device comprising:

15 a substrate (18) having a surface, a barrier film (24) on  
the substrate (18), a material (22) directly on the barrier  
film (24);

20 and characterized in that the barrier film (24) is  
10 comprised of a layer of elemental metal atoms attached to said  
surface.

25 8. A semiconductor device comprising:

a substrate (18), a barrier film (24) on the substrate

30 15 (18), a material (22) directly on the barrier film (24);

and characterized in that the barrier film (24) has a  
thickness less than 100Å.

35 9. A semiconductor device comprising:

20 a substrate material (18) having a surface, a barrier film  
40 (24) on the substrate surface, a conductor (22) directly on the  
barrier film (24), and the conductor (22) having a tendency to  
diffuse into the substrate material (18) if in direct contact  
45 therewith;

25 characterized in that the barrier film (24) has a layer  
comprising elemental metal atoms attached to the substrate  
50 surface surface, and wherein the barrier film layer (24).

5 comprising elemental metal atoms serves as a barrier,  
inhibiting diffusion of the conductor (22) into the substrate  
10 material (18).

15 10. A semiconductor device according to claim 9, wherein the  
barrier film (24) has a thickness of not more than  
approximately 100Å.

20 11. A semiconductor device according to claim 9, wherein the  
10 barrier film (24) has a thickness of not more than  
approximately 20Å.

25 12. A semiconductor device according to claim 9, wherein the  
barrier film (24) has a thickness of not more than  
30 15 approximately 5Å.

35 13. A semiconductor device according to claim 9, wherein the  
monolayer of the barrier film (24) comprises metal atoms  
selected from barium atoms, strontium atoms, cesium atoms, and  
20 rubidium atoms, singly or in combinations thereof, located on  
40 said surface of the substrate (18).

45 14. A semiconductor device according to claim 9, wherein the  
barrier film (24) comprises a plurality contiguous monolayers  
25 (71a-c) of metal atoms located on the surface of the substrate  
material (18).  
50

5 15. A semiconductor device according to claim 9, wherein the  
barrier film (24) comprises a plurality of contiguous  
10 monolayers comprising two or more different types of metal  
atoms selected from the group consisting of barium atoms,  
5 strontium atoms, cesium atoms, and rubidium atoms.

15 16. A semiconductor device according to claim 9, wherein said  
barrier film (24) is a single monolayer attached to said  
20 surface of the substrate material (18).

10 17. A semiconductor device according to claim 9, in which said  
25 substrate material (18) is a semiconductor.

30 18. A semiconductor device according to claim 9, in which said  
15 substrate material (18) is a silicon semiconductor.

35 19. A semiconductor device according to claim 9, in which said  
substrate material (18) is an insulating material.

20 20. A semiconductor device according to claim 9, in which said  
40 substrate material (18) is silicon oxide.

45 21. A semiconductor device according to claim 9, in which the  
conductor (22) is a metal.

25 22. A semiconductor device according to claim 9, in which the  
50 conductor (22) comprises copper.

5

23. A process for making a semiconductor device characterized by the steps of:

10

forming, on a surface (51) of a substrate material (52), a

5 barrier film (54) having a monolayer of metal atoms immediately adjacent the surface (51) of the substrate material (52); and

15

depositing a material (22) directly on the barrier film (54).

20

10 24. A process for making a semiconductor device characterized by the steps of:

25

forming, on a surface (51) of a substrate material (52), a barrier film (54) including a layer of elemental metal atoms attached to said surface (51), and where the barrier film has a

30

15 thickness of less than 100Å; and

depositing a material (22) directly on the barrier film (54).

35

25. A process according to claim 24, where the substrate material (52) is selected as silicon and the material (22) is selected as a conductor material.

40

26. A process according to claim 25, wherein the conductor material (22) comprises copper.

45

25

27. A process according to claim 24, wherein the barrier film (54) has a thickness of not more than approximately 20Å.

50

5

28. A process according to claim 24, wherein the barrier film (54) has a thickness of not more than approximately 5Å.

10

29. A process according to claim 24, wherein the barrier film (54) comprises one or more monolayers of metal atoms.

15

30. A process according to claim 24, wherein said step of forming said barrier film (54) comprises sequentially forming a plurality of contiguous monolayers (71a-c) of metal atoms on said surface (51) of said substrate material (52).

20

25

31. A process according to claim 24, in which the step of forming the barrier film (54) comprises depositing a monolayer precursor compound (50) on the substrate (52) by molecular beam epitaxy, and then annealing the monolayer precursor compound to form a monolayer (54) of metal atoms on the surface (51) of the substrate (52).

30

35

32. A process according to claim 31, wherein the precursor compound (50) is a metal halide.

40

45

33. A process according to claim 31, wherein the precursor compound (50) includes a Group I metal halide.

50

34. A process according to claim 31, wherein the precursor compound (50) includes a Group II metal halide.

50

5 35. A process according to claim 31, wherein the precursor  
compound (50) is a metal halide selected from one or more of  
10  $\text{BaF}_2$ ,  $\text{BaCl}_2$ ,  $\text{SrF}_2$ ,  $\text{SrCl}_2$ ,  $\text{CsF}$ ,  $\text{CsCl}$ ,  $\text{RbF}$ , and  $\text{RbCl}$ .

5 36. A process according to claim 31, wherein the depositing  
and annealing steps are repeated one or more times to form a  
15 plurality of contiguous monolayers (71a-c) on the surface (51)  
of the substrate (52).

20 37. A process according to claim 24, in which the step of  
forming said barrier film (54) comprises depositing a monolayer  
25 precursor compound (50) on said substrate (52) by sputtering,  
and then annealing said monolayer precursor compound (50) to  
form a monolayer (54) of metal atoms on the surface (51) of the  
30 15 substrate (52).

35 38. A process according to claim 37, wherein the precursor  
compound (50) is a metal halide.

40 39. A process according to claim 37, wherein the precursor  
compound (50) includes a Group I metal halide.

45 40. A process according to claim 37, wherein the precursor  
compound (50) includes a Group II metal halide.

25 41. A process according to claim 37, wherein the precursor  
50 compound (50) is a metal halide selected from one or more of

5 BaF<sub>2</sub>, BaCl<sub>2</sub>, SrF<sub>2</sub>, SrCl<sub>2</sub>, CsF, CsCl, RbF, and RbCl.

10 42. A process according to claim 37, wherein the depositing  
and annealing steps are repeated one or more times to form a  
5 plurality of contiguous monolayers (71a-c) on the surface (51)  
15 of the substrate (52).

20 43. A process according to claim 24, in which the step of  
forming said barrier film (54) comprises depositing a monolayer  
10 precursor compound (50) on said substrate (52) by physical  
vapor deposition, and then annealing said monolayer precursor  
25 compound (50) to form a monolayer of metal atoms on the surface  
(51) of the substrate (52).

30 44. A process according to claim 24, in which the step of  
forming said barrier film (54) comprises depositing a monolayer  
precursor compound (50) on said substrate (52) by a deposition  
35 process selected from the group consisting of molecular beam  
epitaxy and physical vapor deposition, and then chemical  
20 etching said monolayer precursor compound (50) to form a  
40 monolayer of metal atoms on the surface (51) of the substrate  
(52).

45 45. A process according to claim 24, in which the substrate  
25 material (52) is a semiconductor material.

5

46. A process according to claim 24, in which the substrate material (52) is silicon semiconductor.

10

47. A process according to claim 24, in which the substrate material (52) is an insulating material.

15

48. A process according to claim 24, in which the substrate material (52) is a silicon oxide.

20

49. A process according to claim 24, in which the conductor (22) is a metallic conductor.

25

50. A process according to claim 24, in which the conductor (22) comprises copper.

30

15

51. The product of the process as recited in claim 23.

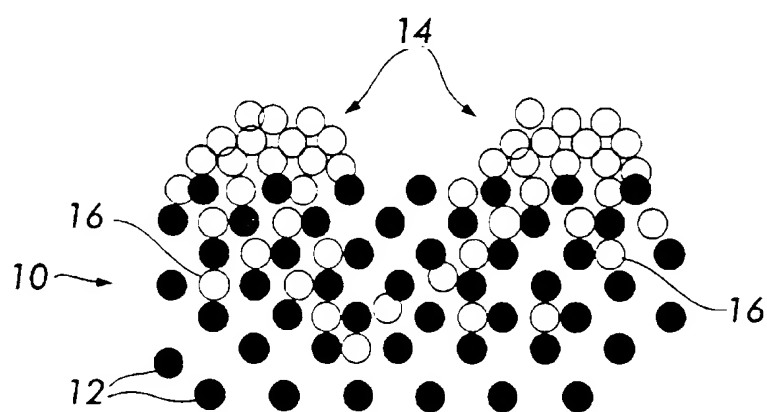
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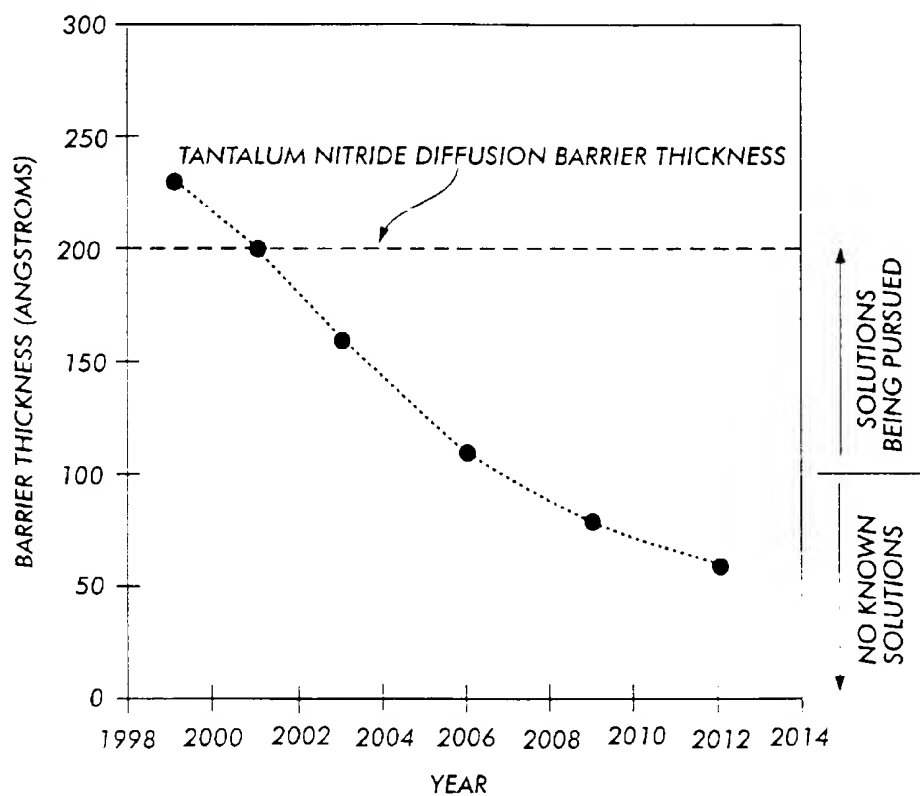
52. The product of the process as recited in claim 24.

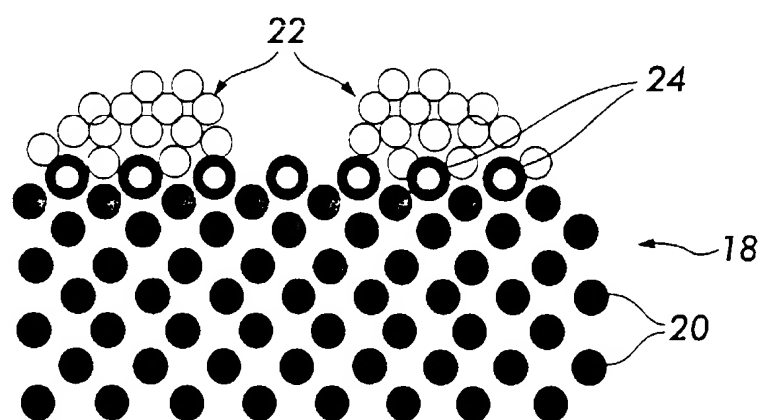
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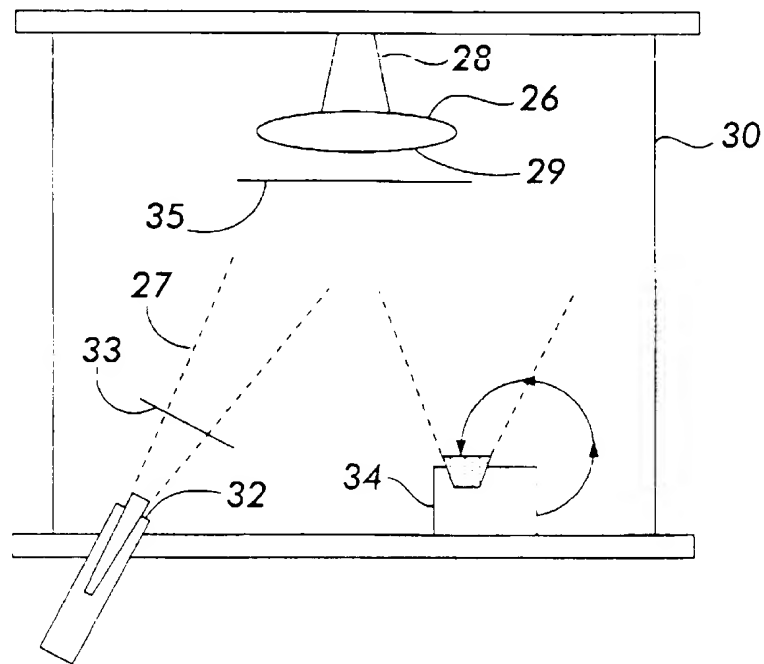
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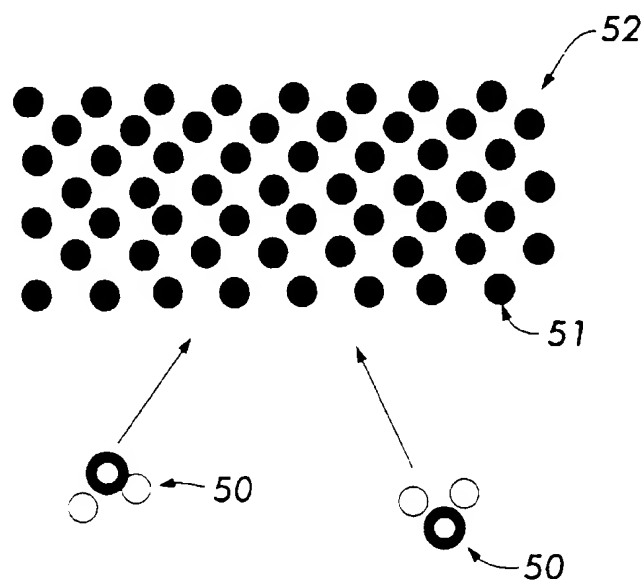
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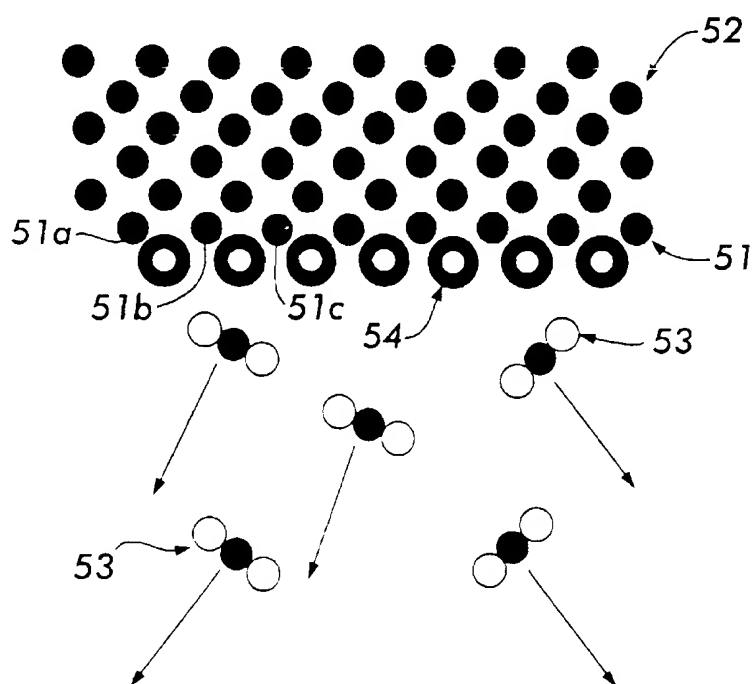
*FIG. 1*

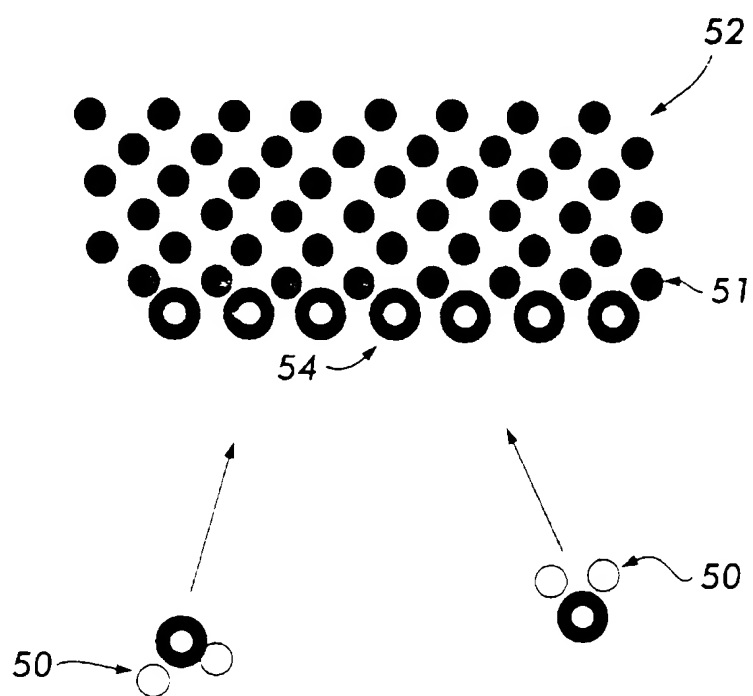
**FIG. 2**

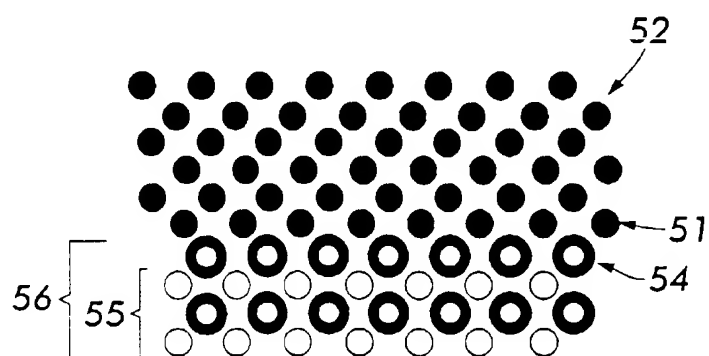
*FIG. 3*

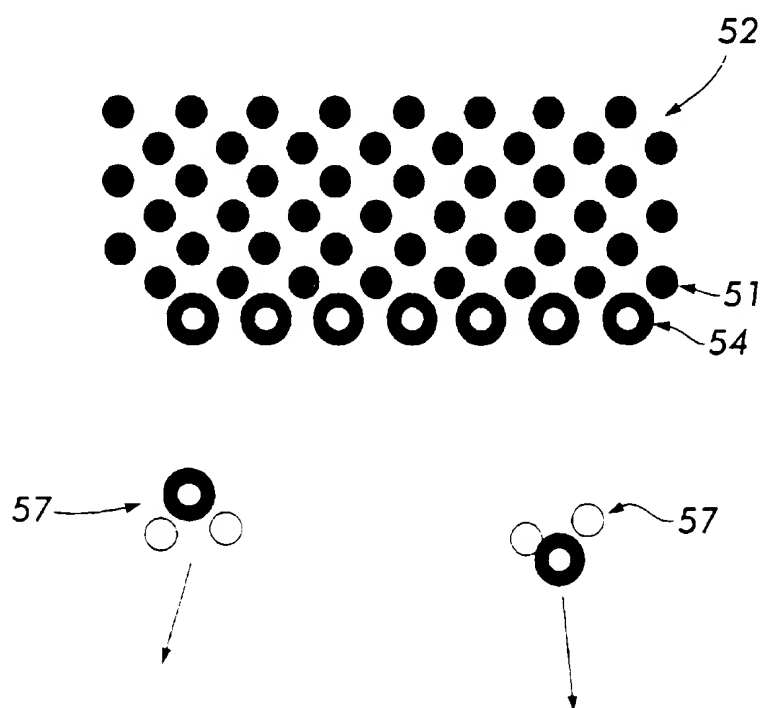
**FIG. 4**

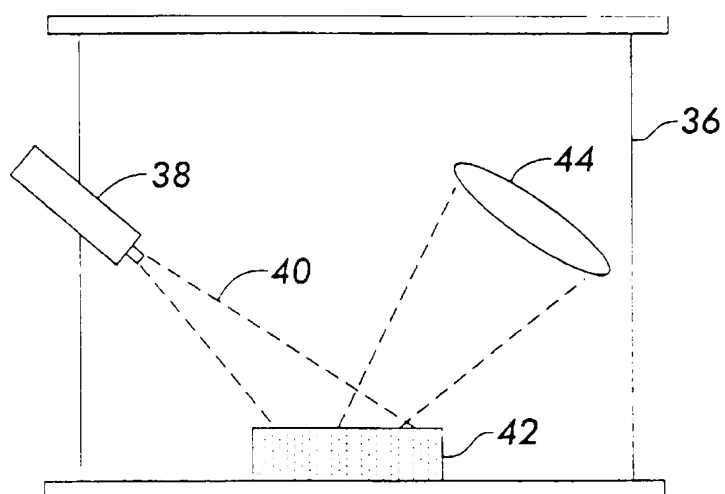
*FIG. 5A*

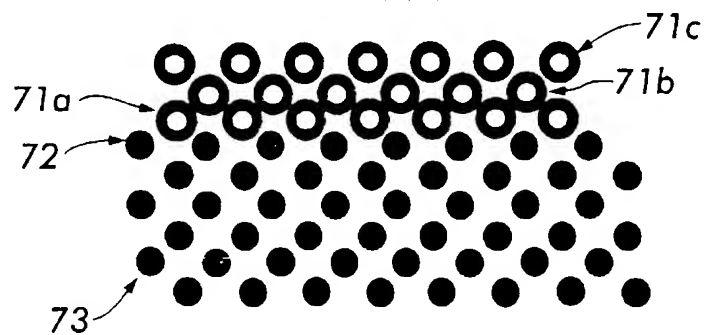
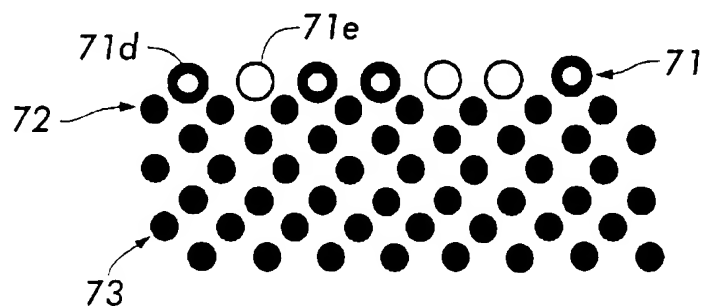
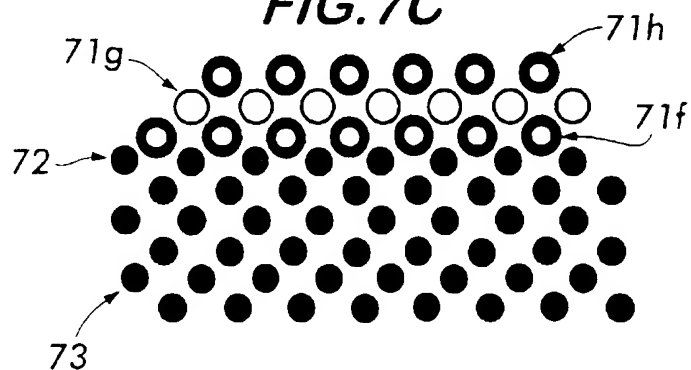
**FIG. 5B**

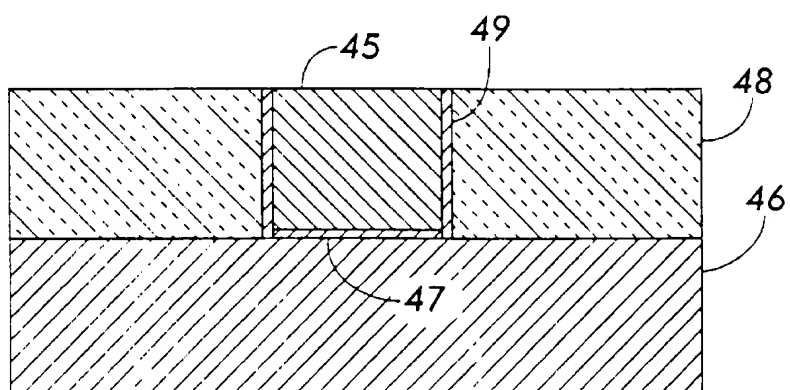
*FIG. 5C*

*FIG. 5D*

*FIG. 5E*

**FIG. 6**

**FIG. 7A****FIG. 7B****FIG. 7C**

**FIG. 8**

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US99/16719

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L 29/43; 21/441

US CL : 438/687, 643; 257/762,767

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/687, 643; 257/762,767

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
NONEElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
NONE

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 6 310 509 A (NONE) 04 NOVEMBER 1994, (04/11/94) abstract	1, 5, 7, 9,, 14, 17-23, 51
X	EP 0 851 483 A (CHEN et al) 01 JULY 1998, (01/07/98) p.4, lines 55-59; p. 5, lines 1 and 15-19.	1, 2, 5, 7-10, 14, 17-26, 29-30, 45-52
X	US 5,637,533 A (CHOI) 10 JUNE 1997, (10/07/97) col. 2, lines 24-51.	1, 2, 5, 7, 9, 14, 17-23, 51
X	US 5,670,420 A (CHOI) 23 SEPTEMBER 1997, (23/09/97) col. 1, lines 63068; col. 2, lines 10-28.	1, 2, 7, 9, 14, 17-24, 51

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents	* T* later documents published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
* A* document defining the general state of the art which is not considered to be of particular relevance	* X* document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
* E* earlier documents published on or after the international filing date	* Y* document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combinations being obvious to a person skilled in the art
* I* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another document or other special reason (as specified)	* A* document member of the same patent family
* O* document referring to an oral disclosure, use, exhibition or other means	
* P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

30 OCTOBER 1999

Date of mailing of the international search report

17 NOV 1999

Name and mailing address of the ISA/US  
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Washington, D.C. 20540

Authorized officer

CARIDAD FERRERAST

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US99/16719

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P	EP 0 881 673 A (ASHLEY, et al) 02 DECEMBER 1998, (02/12/98) col. 8, lines 55-59; col. 9, lines 1-35.	1, 2, 5, 7-10, 17- 24, 45-52
X, P	US 5,824,599 A (SCHACHAM-DIAMAND et al) 20 OCTOBER 1998, (20/10/98) col. 6, lines 35-50	1, 5, 7, 9, 14, 17, 23, 51